FORM PTO-1390 (REV 12-28-99)

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 500.40053X00 filed April 24, 2001

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): 09/830127

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP99/05848	22 October 1999 (22.10.99)	October 29, 1998 (29.10.98)

TITLE OF INVENTION: MULTILAYER ELECTRONIC PART, ITS MANUFACTURING METHOD, TWO-DIMENSIONALLY ARRAYED ELEMENT PACKAGING STRUCTURE, AND ITS MANUFACTURING METHOD

APPLICANT(S) FOR DO/EO/US: ISHIHARA, Shosaku; NAKAMURA, Masato; KUROKI, Takashi

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. [X] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [X] has been transmitted by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. [ ] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [ ] have been transmitted by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A FIRST preliminary amendment.
    [ ] A SECOND or SUBSEQUENT preliminary amendment.
14. [ ] A substitute specification.
15. [X] A change of power of attorney and/or address letter.
16. [X] Other items or information:

International Publication No. WO00/26971 coversheet
International Search Report w/cited references
Information Disclosure Sheet Under 37 CFR 1.56 w/references
Figs. 1A-1D,2A-2D,3A-3C,4A-4D,5A-5B,6A-6D,7A-7G,8A-8D, 9A-9C,10A-10C,11A-11B,12-13,14A-14F,15-16
Credit Card Payment Form
Claim For Priority Letter

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/830127	PCT/JP99/05848	500.40053X00

17. [X] The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

	CALCULATIONS PTO USE ONLY
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$970.00**	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$840.00**	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$690.00**	
International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$670.00**	
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) **$96.00**	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00
Surcharge of **$130.00** for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	16 - 20 =	0	X **$18.00**	$ 0.00
Independent claims	3 - 3 =	0	X **$78.00**	$ 0.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$260.00**	$ 0.00

TOTAL OF ABOVE CALCULATIONS =	$
Reduction of 1/2 for filing by small entity, if applicable. A Small Entity Statement must also by filed (Note 37 CFR 1.9, 1.27, 1.28).	$ 0.00
SUBTOTAL =	$
Processing fee of **$130.00** for furnishing the English translation later than [ ]20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +	$ 0.00
TOTAL NATIONAL FEE =	$
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +	$ 0.00
TOTAL FEES ENCLOSED =	$ 860.00
Amount to be refunded:	$
charged:	$

a. [X] A check in the amount of $ 860.00 to cover the above fees is enclosed.

b. [ ] Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 01-2135. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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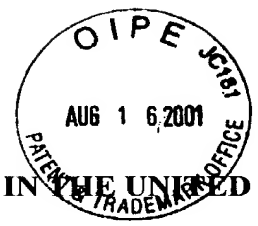
SIGNATURE:

Melvin Kraus
NAME

22,466
REGISTRATION NUMBER



500.40053X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: ISHIHARA et al

Serial No.: 09/830,127

Filed: April 24, 2001

For: Multilayer Electronic Part, Its Manufacturing Method, Two-Dimensionally Arrayed Element Packaging Structure, And Its Manufacturing Method

International Appln. No.: PCT/JP99/05848

International Filing Date: October 22, 1999

ATTN: PCT Branch

RESPONSE TO NOTIFICATION OF DEFECTIVE RESPONSE

Assistant Commissioner
For Patents
Washington, D.C. 20231

August 16, 2001

Sir:

This is in response to the Notification of a Defective Response and the attached Notification of a Defective Oath or Declaration mailed August 8, 2001, in connection with the above-identified application.

The notifications mailed August 8, 2001 indicate that the declaration of the inventors filed July 13, 2001 is not in compliance with 37 CFR 1.497 since it identifies the sixth inventor's name differently than in the international application. This holding is traversed, and it is submitted the declaration is in compliance with 37 CFR 1.497 and should be accepted for the following reasons.

Under 37 CFR 1.497(a)(3), the declaration in a national stage application must

identify each inventor. The declaration submitted July 13, 2001, properly identifies the sixth inventor as Takaya OSAWA. The indication of the sixth inventor's name as Takaya Ohosawa in the International application is merely a typographical or transliteration error in the spelling of the name. The spelling is correct in the declaration submitted July 13, 2001. Therefore, the declaration complies with the requirements of 37 CFR 1.497 and should be accepted.

It is noted that when a typographical or transliteration error in the spelling of an inventor's name is discovered during the pendency of the application, a petition is not required, nor is a new oath or declaration needed. Manual of Patent Examining Procedure (MPEP) 605.04(b). Instead, the Patent and Trademark Office should simply be notified of the error. Here the typographical or transliteration error in the spelling of the sixth inventor's name is in the international application. It is requested that the Patent and Trademark Office simply note the same and correct the sixth inventor's name to that given in the declaration filed July 13, 2001, i.e., to Takaya OSAWA.

For the foregoing reasons, the declaration submitted July 13, 2001 complies with the requirements of 37 CFR 1.497 and should be accepted.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 500.40053X00), and

please credit any excess fees to such deposit account.

Respectfully submitted,

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DESCRIPTION

MULTILAYER ELECTRONIC PART, ITS MANUFACTURING METHOD, TWO-DIMENSIONALLY ARRAYED ELEMENT PACKAGING STRUCTURE, AND ITS MANUFACTURING METHOD

TECHNICAL FIELD

The present invention relates to a multilayer electronic part, its manufacturing method, a two-dimensionally arrayed element packaging structure and its manufacturing method, or in particular a technique for a probe having a multiplicity of two-dimensionally arrayed piezoelectric ceramic transducer elements (multilayer electronic part) suitably used, for example, to attain a high performance of an ultrasonic probe apparatus.

BACKGROUND ART

In recent years, an ultrasonic transceiver using a piezoelectric ceramic transducer element has come to be used for various applications. Especially, the ultrasonic diagnostic system which, unlike the X-ray diagnosis, permits the interior of the human body to be observed without adversely affecting the human body has extended widely as medical equipment. The ultrasonic diagnostic system used for the ultrasonic diagnosis method uses a probe having a multiplicity of piezoelectric ceramic transducer elements as an

ultrasonic transceiver. The probe configured with piezoelectric ceramic transducer elements includes a scanning probe having a multiplicity of minuscule piezoelectric ceramic transducer elements arranged for diagnosing the interior of the human body by forming tomographic images.

Among these probe structures, with the probe having one-dimensionally arranged piezoelectric ceramic transducer elements, the focal point can be arbitrarily set at a near or far point from the probe by selecting the number of elements arranged in a given direction, while the focal point is fixed in the direction orthogonal to the particular direction, and therefore a clear image cannot be produced in other than the range corresponding to the depth of focus.

In order to solve the disadvantage described above, a two-dimensionally arrayed probe structure having piezoelectric ceramic transducer elements arranged not only in a single direction but also in the direction orthogonal thereto has been developed. Such a probe structure is described, for example, in "1996, IEEE Ultrasonics Symposium, pp. 1523-1526". With this two-dimensional probe structure, a key to achieving a high performance is how the piezoelectric ceramic transducer elements are reduced in size and how densely they are arranged in a limited space. Along with the high-density arrangement, it is important that each of the two-dimensionally arrayed piezoelectric ceramic

transducer elements and the electrical connections thereof are free of a defect, i.e. each piezoelectric ceramic transducer element making up the probe is free of a defect.

From this viewpoint, a method of configuring two-dimensionally arranged probe structure configured of modules each having a plurality of elements is described in "1996 IEEE Ultrasonics Symposium, pp. 1573-1576". This publicly known reference discloses a method of constructing a probe structure having 4096 (64 x 64) elements of 0.22 mm x 0. 22 mm as a combination of a plurality of modules each including two columns of 64 elements.

The conventional modular structure disclosed in the aforementioned reference, however, is so configured that a flexible wiring board and a common electrode are connected to the surface of each piezoelectric ceramic transducer element to drive the particular piezoelectric ceramic transducer element. Thus, the elements are not structured independently of each other but bonded to each other. A defective or ill-connected element, if included in the elements that have built up a module, therefore, cannot be independently replaced or the connection failure thereof cannot be repaired easily, thereby leading to the problem of a low yield for each module.

Also, the conventional modular structure presupposes that each piezoelectric ceramic transducer

element is configured of a single board (single layer), and no consideration is given of the application to a multilayer piezoelectric ceramic transducer element required for improving the probe performance.

Further, the conventional multilayer piezoelectric ceramic transducer element configured either in such a manner that as shown in Fig. 15, alternate ones of a surface electrode 12, an internal electrode 13' in ceramics 11 and a back electrode 15 along the thickness of the multilayer are electrically connected to each other by side electrodes 61 formed on the two opposed side surfaces of the element, or in such a manner that as shown in Fig. 16, alternate ones of the surface electrode 12, the internal electrode 13' and the back electrode 15 are electrically connected to each other alternately along the thickness of the multilayer by a conductive material 62 filled in a through hole. As a result, the production process is comparatively complicated and the size reduction is limited. Also, for connecting the two electrode groups of the element to an external means, the two surfaces of the element are unavoidably used for external connection. Thus, it is difficult to replace the element or repair the connection, thereby making the application to the probe unsuitable.

The present invention has been developed in view of this point, and the object thereof is to provide a two-dimensionally arrayed probe (element

packaging structure) in which a multilayer element can be used as a piezoelectric ceramic transducer element and each defective element, if any, can replaced or any ill connection of each element can be repaired on the one hand, and to provide a piezoelectric ceramic transducer element (multilayer electronic part) suitable for realizing such an element packaging structure on the other hand.

DISCLOSURE OF INVENTION

In order to achieve the object described above, according to this invention, a multilayer electronic part is configured with, for example, a multilayer chip-like element having a surface electrode, an internal electrode and a back electrode and a flexible board attached to one side surface of the chip-like element, alternate ones of the electrodes along the thickness of the multilayer of the chip-like element are connected electrically to each other by electrode patterns of the flexible board thereby to form two electrode groups, and the end portions of the electrode patterns of the flexible board, for example, are used as two electrode portions for external connection which are electrically connected with the two electrode groups. A plurality of the aforementioned multilayer electronic parts are arranged in columns and rows and integrated into a two-dimensionally arrayed module. As many modules as

required are combined to construct a probe for an ultrasonic probe apparatus.

The use of the multilayer piezoelectric ceramic transducer element (the multilayer electronic part described above) makes it possible to produce a compact, high-performance probe. Also, in view of the configuration in which each multilayer electronic part (piezoelectric ceramic transducer element) is provided with two independent electrode portions for external connection, each multilayer electronic part (piezoelectric ceramic transducer element) can be inspected for a defective chip-like element and a connection failure. Thus a defective multilayer electronic part can be replaced and the ill connection of each multilayer electronic part can be repaired easily for each piezoelectric ceramic transducer element (multilayer electronic part). As a result, the defective module is eliminated and a high-yield module production is made possible. Further, the connection for forming two electrode groups of a chip-like element and the formation of electrode portions for external connection are performed by the electrode patterns of the flexible board on one side surface of the chip-like element. Therefore, the production process is simplified and the multilayer electronic part (piezoelectric ceramic transducer element) can be remarkably reduced in size.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 is a diagram for explaining a multilayer electronic part (piezoelectric ceramic transducer element) according to a first embodiment of the present invention.

Fig. 2 is a diagram for explaining a multilayer electronic part (piezoelectric ceramic transducer element) according to a second embodiment of the present invention.

Fig. 3 is a diagram for explaining a multilayer electronic part (piezoelectric ceramic transducer element) according to a third embodiment of the present invention.

Fig. 4 is a diagram for explaining a multilayer electronic part (piezoelectric ceramic transducer element) according to a fourth embodiment of the present invention.

Fig. 5 is a diagram for explaining a multilayer electronic part (piezoelectric ceramic transducer element) according to a fifth embodiment of the present invention.

Fig. 6 is a diagram for explaining a multilayer electronic part (piezoelectric ceramic transducer element) according to a sixth embodiment of the present invention.

Fig. 7 is a diagram for explaining an example of a method for manufacturing a multilayer electronic part and a method for manufacturing a two-dimensionally

arrayed element packaging structure using the former manufacturing method according to an embodiment of the present invention.

Fig. 8 is a diagram for explaining a multilayer electronic part (piezoelectric ceramic transducer element) according to a seventh embodiment of the present invention. Fig. 9 is a diagram for explaining a multilayer electronic part (piezoelectric ceramic transducer element) according to an eighth embodiment of the present invention.

Fig. 10 is a diagram for explaining a multilayer electronic part (piezoelectric ceramic transducer element) according to a ninth embodiment of the present invention.

Fig. 11 is a diagram for explaining a multilayer electronic part (piezoelectric ceramic transducer element) according to a tenth embodiment of the present invention.

Fig. 12 is a diagram for explaining an electronic part (piezoelectric ceramic transducer element) of single layer type according to an 11th embodiment of the present invention.

Fig. 13 is a diagram for explaining an electronic part (piezoelectric ceramic transducer element) of a single layer type according to a 12th embodiment of the present invention.

Fig. 14 is a diagram for explaining another example of a method for manufacturing a multilayer

electronic part and a method for manufacturing a two-dimensionally arrayed element packaging structure using the former manufacturing method according to an embodiment of the present invention.

Fig. 15 is a diagram for explaining an example of a conventional multilayer electronic part (piezoelectric ceramic transducer element).

Fig. 16 is a diagram for explaining another example of a conventional multilayer electronic part (piezoelectric ceramic transducer element).

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiments of the invention will be explained below with reference to the drawings.

Fig. 1 is a diagram showing a multilayer electronic part (piezoelectric ceramics transducer element according to a first embodiment of the invention. In this diagram, 1 designates a multilayer chip-like element, 11 ceramics, 12 a surface electrode, 13 a first internal electrode, 14 a second internal electrode, 15 a back electrode, 16 insulation patterns, 17 conductor patterns and 18 a protective insulating film.

In the chip-like element 1 of multilayer type according to the embodiments of the invention including this embodiment, as shown in (a) of Fig. 1, a ceramics 11 is laid in multiple layers with the internal electrodes 13, 14 therebetween, and the surface

electrode 12 and the back electrode 15 are formed on the front and back surface, respectively. Also, the planar shape of all the electrodes is formed equally to the planar shape of the ceramics 11. On the four side surfaces of the chip-like element 1, therefore, the end surfaces of the surface electrode 12, the first internal electrode 13, the second internal electrode 14 and the back electrode 15 is exposed on a single surface.

In the chip-like element 1 having this basic configuration, according to this embodiment, the insulation patterns 16 are formed in such a manner that only a part of the first internal electrode 13 and a part of the second internal electrode 14 are exposed on one side surface of the chip-like element 1, as shown in (b) of Fig. 1. After that, as shown in (c) of Fig. 1, alternate ones of the electrodes 12 to 15 along the thickness of the multilayer are electrically connected to each other by the conductor patterns 17 (in the case under consideration, the surface electrode 12 and the second internal electrode 14 are connected to each other, and the first internal electrode 13 and the back electrode 15 are connected to each other). Then, as shown in (d) of Fig. 1, the side surface of the chip-like element 1 on which the electrodes are connected in a predetermined relation is covered with a protective insulating film 18 thereby to complete a multilayer electronic part. According to this embodiment, the

surface electrode 12 and the back electrode 15 function also as electrodes for external connection.

In a multilayer electronic part having this configuration, alternate ones of the electrodes 12 to 15 along the thickness of the multilayer of the chip-like element 1 are connected to each other on one side surface of the chip-like element 1. Therefore, the same planar shape can be obtained for all the electrodes 12 to 15, and as compared with the conventional structure shown in Figs. 15 and 16, the internal electrode can be formed and the multilayer can be positioned easily (the manufacturing process is simplified), and the size can be minimized.

Fig. 2 is a diagram showing a multilayer electronic part according to a second embodiment of the invention. In this drawing, the component parts equivalent to those of the aforementioned embodiment are designated by the same reference numerals, respectively, and will not be described except when required (this also applies to the following described embodiments). In Fig. 2, 19 designates an Ag paste, 20 a flexible board, and 21, 22 a pair of electrode patterns formed on the flexible board.

According to this embodiment, as shown in (a) of Fig. 2, a insulation pattern 16 is formed except for the connecting portions of the electrodes 12 to 15 with the flexible board 20, as shown in (b) of Fig. 2, on one side surface of the chip-like element 1 having a

similar configuration to the one described above. Then, as shown in (c) of Fig. 2, the electrode patterns 21, 22 of the flexible board 20 are connected electrically to the corresponding exposed portions of the electrodes 12 to 15 by the Ag paste 19. In this way, alternate ones of the electrodes 12 to 15 along the thickness of the multilayer are electrically connected (in the case under consideration, the surface electrode 12 and the second internal electrode 14 are connected to each other by the electrode pattern 21 of the flexible board 20, and the first internal electrode 13 and the back electrode 15 are connected to each other by the electrode pattern 22 of the flexible board 20). Incidentally, (c) of Fig. 2 constitutes a side view as related to (b) of Fig. 2, and (d) of Fig. 2 shows the pattern formed surface of the flexible board 20.

As described above, according to this embodiment, the chip-like element 1 and the flexible board 20 make up a multilayer electronic part, and the surface electrode 12 and the back electrode 15 function as electrodes for external connection. The Ag paste 19 used for connecting the chip-like element 1 and the flexible board 20 may be formed on either the chip-like element 1 or the flexible board 20.

This embodiment configured as described above has a similar effect to the first embodiment. Also, since alternate ones of the electrodes 12 to 15 along

the thickness of the multilayer of the chip-like element 1 are connected by the flexible board 20, the production process is simplified.

Fig. 3 is a diagram showing a multilayer electronic part according to a third embodiment of the invention. In this diagram, 23 designates an insulation pattern formed on the flexible board 20.

This embodiment is different from the second embodiment in that unlike in the second embodiment in which the insulation pattern 16 for making possible selective connection is formed on the chip-like element 1, the insulation pattern 23 making possible selective connection is formed on the pattern formed surface of the flexible board 20. The other points are similar to the corresponding ones of the second embodiment. Incidentally, (b) of Fig. 3 represents a somewhat enlarged side view as related to (a) of Fig. 3 in the case where the surface of the chip-like element 1 shown in (a) of Fig. 3 constitutes a connecting surface, and (c) of Fig. 3 shows a pattern formed surface of the flexible board 20.

Also this embodiment having the aforementioned configuration has an effect similar to that of the second embodiment.

The insulation pattern and the conduction pattern described above can be formed either by a thick film method in which a paste is screen-printed to form a pattern or by a thin film method in which a pattern

is formed by depositing by evaporation, sputtering or etching.

Further, the electrical connecting portion of the chip-like element 1 for connection with the electrode pattern of the flexible board 20 may be either an electrode exposed portion of the chip-like element 1 or a conductor pattern portion formed of a thick or thin film on the electrode of the chip-like element 1. The electrical connecting portion of the flexible board 20 for connection with the electrode of the chip-like element 1, on the other hand, may be either an electrode pattern itself of the flexible board 20 or a conductor pattern portion formed of a thick film on the electrode patter of the flexible board 20.

Fig. 4 is a diagram showing a multilayer electronic part according to a fourth embodiment of the invention. In this diagram, 24 designates plated film portions formed on the electrode exposed portion of the chip-like element 1, and 25 a connecting solder.

This embodiment is different from the third embodiment in that, as shown in (a) of Fig. 4, the plated film portion 24 is formed on each of the electrodes 12 to 15 as shown in (b) of Fig. 4 on one side surface of the chip-like element 1 having a similar configuration and in that the solder 25 formed on the chip-like element 1 or the flexible board 20 is used as shown in (c) of Fig. 4 for electrically

connecting the chip-like element 1 and the flexible board 20. The other points are similar to the corresponding points of the third embodiment. Incidentally, (c) of Fig. 4 is a somewhat enlarged side view as related to (b) of Fig. 4, and (d) of Fig. 4 shows a pattern formed surface of the flexible board 20.

This embodiment having the aforementioned configuration has a similar effect to the second embodiment.

Fig. 5 is a diagram showing a multilayer electronic part according to a fifth embodiment of the invention. In this diagram, 26 designates an anisotropic conductive film.

This embodiment is different from the fourth embodiment in that as shown in (a) of Fig. 5, the anisotropic conductive film 26 is used for connecting the chip-like element 1 and the flexible board 20 electrically to each other, and the remaining points are similar to the fourth embodiment. Incidentally, (b) of Fig. 5 shows a pattern formed surface of the flexible board 20.

This embodiment having the above-mentioned configuration has a similar effect to the second embodiment.

Incidentally, the chip-like element 1 and the flexible board 20 can be electrically connected to each other not only by the aforementioned means but also by

such a method as wire bonding or metal diffusion connection method.

Fig. 6 is a diagram showing a multilayer electronic part according to a sixth embodiment of the invention. In the diagram, 27 designates electrode pads formed through the flexible board 20.

This embodiment is different from the fourth embodiment in that as shown in (c) and (d) of Fig. 6, the electrode pads 27, 27 exposed on the side of the flexible board 20 far from the pattern formed surface thereof and connected to the electrode patterns 21, 22, respectively, of the flexible board 20, constitute electrodes for external connection. The other points are similar to the corresponding points of the fourth embodiment.

The present embodiment having this configuration has a similar effect to the second embodiment. Further, the present embodiment has the effect of facilitating the external connection of the multilayer electronic part in view of the fact that the electrode pair for external connection can be concentrated on one side surface of the multilayer electronic part.

Now, a method of manufacturing the multilayer electronic part described above and an example of a method of manufacturing a two-dimensionally arrayed element packaging structure using the former method will be explained with reference to Fig. 7. Fig. 7

shows a method of manufacturing a multilayer electronic part corresponding to the fourth embodiment of Fig. 4 and a method of manufacturing a two-dimensionally arrayed element packaging structure using the multilayer electronic part.

First, as shown in (b) of Fig. 7, a bar-shaped subbase member 31 as wide as one chip is cut out from a tabular chip-like base member 30 as shown in (a) of Fig. 7. Then, as shown in (c) of Fig. 7, a plated film portion 24 is formed on the end surface of each of the electrodes 12 to 15 exposed to a predetermined long side surface of the base member 31 thus cut out.

As shown in (d) of Fig. 7, on the other hand, the flexible board base member 32 having a multiplicity of electrode pattern pairs 21, 22 is formed with an insulation pattern making selective connection possible, after which a connecting solder 25 is formed at each portion of the electrode patterns 21, 22 exposed from the insulation pattern 23.

Then, as shown in (e) of Fig. 7, the connecting surfaces of the bar-shaped subbase member 31 and the flexible board base member 32 are attached close to each other in position and heat treated thereby to electrically connect the connecting points of the subbase member 31 and the flexible board base member 32 to each other. After that, a minuscule gap (10 to several tens of μm) between the subbase member 31 and the flexible board base member 32 is filled with

an insulating adhesive (such as a urethane resin adhesive of low viscosity), so that the subbase member 31 and the flexible board base member 32 are mechanically firmly connected to each other.

Then, as shown in (f) of Fig. 7, each multilayer electronic part 33 is cut out by dicer from the integrated base member including the subbase member 31 and the flexible board base member 32 thereby to complete the multilayer electronic parts 33.

Each multilayer electronic part 33 completed through the processes described above is inspected, and as shown in (g) of Fig. 7, a predetermined number of acceptable multilayer electronic parts 33 are combined in columns and rows and integrated by the resin 34. In this way, a module 35 is produced for a two-dimensionally arrayed probe. A multiplicity of the modules 35 are combined to complete a two-dimensionally arrayed probe.

The two-dimensionally arrayed probe produced by combining the modules 35 as described above can reduce the size of each multilayer electronic part and thus can reduce the whole size. Nevertheless, the external connection of each multilayer electronic part requires considerable tact. The external connection is easy and accurate advantageously for a multilayer electronic part (or an electronic part of single layer type) having such configuration that a pair of electrodes for external connection are arranged on the

extension of the flexible board attached to the side surface of the chip-like element as described below.

Fig. 8 is a diagram showing a multilayer electronic part according to a seventh embodiment of the invention. This embodiment is an example of a development from the second embodiment shown in Fig. 2.

This embodiment is different from the second embodiment in that an extension 20a is formed on the flexible board 20 connected to one side surface of the chip-like element 1, and the end portions of the electrode patterns 21, 22 of the flexible board 20 for electrically connecting alternate ones of the electrodes 12 to 15 along the thickness of the multilayer of the chip-like element 1 are constituted of the electrode portions 21a, 22a for external connection. The remaining points are similar to those of the second embodiment.

In the multilayer electronic part according to this embodiment having the above-mentioned configuration, alternate ones of the electrodes 12 to 15 along the thickness of the multilayer of the chip-like element 1 are connected to each other on one side surface of the chip-like element 1, and therefore all the electrodes 12 to 15 have the same planar shape. As compared with the conventional structure shown in Figs. 15 and 16, therefore, the formation of the internal electrode can be formed and the multilayer positioning are facilitated (the production process is simplified),

while at the same time minimizing the size. In addition, alternate ones of the electrodes 12 to 15 along the thickness of the multilayer of the chip-like element 1 are connected by the flexible board 20, which is another contributing factor to a simplified production process. Further, in view of the fact that the extension 20a is formed on the flexible board 20, and the end portions of the electrode patterns 21, 22 on the extension 20a constituting the electrode portions 21a, 22a for external connection are led out in the same direction, the external connection of the multilayer electronic parts is facilitated and assured. Even in the case where a multiplicity of multilayer electronic parts are combined into a module, therefore, the superior connection performance is exhibited to the full. Furthermore, the ill connection of the multilayer electronic parts can be individually handled easily, thereby making possible replacement and repair easier and more accurate.

Fig. 9 is a diagram showing a multilayer electronic part according to an eighth embodiment of the invention. This embodiment is an example of a development from the this embodiment shown in Fig. 3. This embodiment is different from the third embodiment in that an extension 20a is formed on the flexible board 20 and the portions of the electrode patterns 21, 22 on the extension 20a constitute the electrode portions 21a, 22a for external connection. The

remaining points are similar to the corresponding points of the third embodiment.

This embodiment having the aforementioned configuration has the same effect as the seventh embodiment.

Fig. 10 is a diagram showing a multilayer electronic part according to a ninth embodiment of the invention. This embodiment is an example of a development from the fourth embodiment described above. This embodiment is different from the fourth embodiment in that an extension 20a is formed on the flexible board 20, and the portions of the electrode patterns 21, 22 of the flexible board 20 on the extension 20a constitute the electrode portions 21a, 22a for external connection. The remaining points are similar to the corresponding points of the fourth embodiment.

The present embodiment having this configuration has a similar effect to the seventh embodiment.

Fig. 11 is a diagram showing a multilayer electronic part according to a tenth embodiment of the invention. This embodiment is an example of a development from the fifth embodiment described above. This embodiment is different from the fifth embodiment in that an extension 20a is formed on the flexible board 20, and the portions of the electrode patterns 21, 22 on the extension 20a constitute the electrode portions 21a, 22a for external connection. The

remaining points are similar to the corresponding points of the fourth embodiment.

The present embodiment having this configuration has a similar effect to the seventh embodiment.

The first to tenth embodiments described above represent an example of the multilayer electronic part with a multiplicity of ceramic layers laid one on another. Now, an explanation will be given of an application to a piezoelectric ceramic transducer element of a single plate type having a single layer of ceramics.

Fig. 12 is a diagram showing an electronic part (piezoelectric ceramics transducer element) according to an 11th embodiment of the invention. In this diagram, 41 designates a chip-like element of single layer (single plate) type. The single-plate ceramics 11 is formed with a surface electrode 12 and a back electrode 15. An insulation pattern 16 and a plated film portion 24 are formed selectively on the surface electrode 12 and the back electrode 15 on one side surface of the chip-like element 41. The plated film portion 24 is electrically connected to the corresponding electrode patterns 21, 22 of the flexible board 20 by a solder 25. An extension 20a is formed on the flexible board 20, and the portions of the electrode patterns 21, 22 on the extension 20a function as the electrode portions 21a, 22a for external

connection.

The present embodiment having this configuration represents a piezoelectric ceramic transducer element of single layer (single plate) type, and therefore is inferior in performance to that of the piezoelectric ceramic transducer element of multilayer type. Nevertheless, the multilayer electronic part can be easily and positively connected externally in view of the fact that the flexible board 20 has an extension 20a and the end portions of the electrode patterns 21, 22 of the flexible board 20 on the extension 20a constitute the electrode portions 21a, 22a for external connection and are led out in the same direction. In the case where a multiplicity of multilayer electronic parts are combined into a module, therefore, the superior connection performance is exhibited to the full. Further, ill connection of the multilayer electronic part can be handled individually with ease, thereby facilitating positive replacement or repair.

Fig. 13 is a diagram showing an electronic part (piezoelectric ceramic transducer element) according to a 12th embodiment of the invention. This embodiment is different from the 11th embodiment in that unlike in the 11th embodiment having an insulation pattern 16 on the chip-like element 41 of single layer (single plate) type, the 12th embodiment is formed with an insulation pattern 23 on the flexible board 20. The remaining points are similar to the corresponding ones

of the 11th embodiment.

Also the present embodiment having this configuration exhibits a similar effect to the 11th embodiment.

The multilayer electronic part (piezoelectric ceramics transducer element) shown in the first to tenth embodiments has three layers of ceramics. However, the number of layers of ceramics in the multilayer electronic part according to this invention is not limited and arbitrary.

In the case where a multilayer electronic part or an electronic part is constituted of a chip-like element and a flexible board as shown in the second to 12th embodiments described above, the solder, the thermoplastic paste or the anisotropic conductive sheet or the like arbitrary means can be employed for electrical connection between the chip-like element and the flexible board as described above. Nevertheless, for securing the mechanical strength, it is preferable to fill an insulating adhesive (such as an urethan resin adhesive of low viscosity) in the minuscule gap between the chip-like element and the flexible board.

Now, an example of a method of manufacturing a multilayer electronic part so configured that the electrode portions 21a, 22a for external connection are arranged on the extension 20a of the flexible board 20 described above and an example of a method for manufacturing a two-dimensionally arrayed element

packaging structure using the multilayer electronic part will be explained below with reference to Fig. 14.

First, as shown in (a) of Fig. 14, a tabular sound matching layer 45 and a tabular sound attenuation layer 46 are fixedly integrated above and under a tabular chip-like element base member 30 to prepare a chip-like element composite base member 47. Then, as shown in (b) of Fig. 14, a bar-shaped subcomposite base member 48 as wide as one chip is cut out from the chip-like element composite base material 47.

Then, as shown in (c) of Fig. 14, Ni is plated on the end surfaces of the electrodes 12 to 15 exposed to a predetermined longitudinal side surface of the bar-shaped subcomposite base member 48 thus cut out, and Au is plated on the surface of the Ni plating thereby to form plated film portions 24.

On the other hand, as shown in (d) of Fig. 14, the flexible board base member 49 including a multiplicity of electrode pattern pairs 21, 22 is formed with an insulation pattern for making possible selective connection, after which the portions of the electrode patterns 21, 22 exposed from the insulation pattern are formed with a connecting solder 25. At the same time, the extension 49a of the flexible board base member 49 are formed with electrode portions 21a, 22a for external connection which are connected with the mating electrode patterns 21, 22, respectively. The connecting surfaces of the bar-shaped subcomposite base

member 48 and the flexible board base member 49 are closely attached to each other in position and heat treated. In this way, the connectors of the subcomposite base member 48 and the flexible board base member 49 are electrically connected to each other. After that, the minuscule gap (10 to several tens of μm) between the subcomposite base member 48 and the flexible board base member 49 is filled with an insulative adhesive (such as an urethane resin adhesive of low viscosity) thereby to firmly connect the subcomposite base member 48 and the flexible board base member 49 mechanically to each other.

Then, as shown in (e-1) and (e-2) of Fig. 7, each multilayer electronic part 50 is cut out by dicer from the integrated base member of the subcomposite base member 48 and the flexible board base member 49, thereby completing a multilayer electronic part (ceramic transducer element) 50 with the sound matching layer 45 and the sound attenuation layer 46.

The multilayer electronic parts 50 completed through the processes described above are inspected, and as shown in (f) of Fig. 14, a predetermined number of acceptable ones of the multilayer electronic parts 50 are combined in columns and rows and integrated by resin 51 thereby to fabricate a module 52 for a two-dimensionally arrayed probe. Then, each multilayer electronic part 50 of the module 52 is inspected. With a structure in which the electrodes are connected by

one side surface of each multilayer electronic part 50 and by the use of the solder, the thermoplastic paste or the anisotropic conductive sheet for the connectors, as described above, each defective element can be replaced or the ill connection of each element can be repaired easily like in the normal semiconductor device such as LSI.

Finally, a two-dimensionally arrayed probe is completed by combining a multiplicity of acceptable ones of the modules 52. In this example, a two-dimensionally arrayed probe is produced by arranging 64 modules 52 as elements each including 64 x 64 multilayer electronic parts 50 arranged in 15 mm x 15 mm.

The example shown in Fig. 14 refers to the multilayer piezoelectric ceramic element (multilayer electronic part), and a two-dimensionally arrayed probe can of course be produced by a similar method with a single-layer piezoelectric ceramic element (single-layer electronic part) shown in Figs. 12 and 13.

Also, the bonding of the sound matching layer and the sound attenuation layer is not specifically limited to the production process of Fig. 14, but the sound matching layer and the sound attenuation layer may be fixedly attached to the multilayer piezoelectric ceramic elements (multilayer electronic parts) after being aligned in matrix.

As described above, according to this

invention, a multilayer element can be used as a piezoelectric ceramic transducer element, and a two-dimensionally arrayed probe (element packaging structure) can be realized in which each element can be replaced or the ill connection of each element can be repaired. Also, a piezoelectric ceramic transducer element (multilayer electronic part) can be provided which is suitable for realizing such an element packaging structure.

INDUSTRIAL APPLICABILITY

As described above, according to this invention, a multilayer electronic part is configured of a multilayer chip-like element having a surface electrode, an internal electrode and a back electrode on the one hand and a flexible board attached to one side surface of the chip-like element on the other hand, wherein alternate ones of the electrodes along the thickness of the multilayer of the chip-like element are electrically connected to each other by an electrode pattern of the flexible board thereby to form two electrode groups, and the end portions of the electrode pattern of the flexible board are used as two electrode portions for external connection which are electrically connected to the two electrode groups. Thus, a two-dimensionally arrayed probe (element packaging structure) is provided in which a multilayer element can be used as a piezoelectric ceramic

transducer element and each defective element can replaced or the ill connection of each element can be repaired. Also, a multilayer electronic part is provided which is suitable for realizing such an element packaging structure.

CLAIMS

1. A multilayer electronic part having a surface electrode, an internal electrode and a back electrode, wherein alternate ones of the electrodes along the thickness of the multilayer are electrically connected to each other thereby to constitute two electrode groups, the multilayer electronic part having two electrode portions for external connection which are electrically connected with said two electrode groups, characterized in that said two electrode groups are electrically connected on one side surface of said multilayer electronic part.

2. A multilayer electronic part as described in Claim 1, characterized in that said multilayer electronic part is configured with a chip-like element and a flexible board attached to one side surface of said chip-like element, and alternate ones of the electrodes along the thickness of the multilayer of said chip-like element are connected to each other by an electrode pattern of said flexible board thereby to constitute said two electrode groups.

3. A multilayer electronic part as described in Claim 2, characterized in that an insulative adhesive is filled in the minuscule gap between said chip-like element and said flexible board.

4. A multilayer electronic part as described in Claim 2, characterized in that said two electrode portions for external connection are formed on one side

surface of said chip-like element or the extension of said one side surface.

5. A multilayer electronic part as described in Claim 4, characterized in that said two electrode portions for external connection are formed of the end portions of a pair of said electrode patterns of said flexible board.

6. A multilayer electronic part as described in Claim 2, characterized in that each of said electrodes of said chip-like element and said electrode pattern of said flexible board are connected to each other by a thick film conductive paste or a solder or an anisotropic conductive sheet.

7. A multilayer electronic part as described in Claim 2, characterized in that an insulation pattern for cutting off the conduction between adjacent electrodes along the thickness of the multilayer of said chip-like element is formed on said chip-like element or said flexible board.

8. A method of manufacturing a multilayer electronic part configured with a chip-like element having a surface electrode, an internal electrode and a back electrode and a flexible board attached to one side surface of said chip-like element, wherein alternate ones of the electrodes along the thickness of a multilayer of said chip-like element are electrically connected to each other by an electrode pattern of said flexible board thereby to constitute two electrode

groups, and two electrode portions for external connection which are electrically connected with said two electrode groups are formed of the electrode pattern of said flexible board or a conductive portion connected to said electrode pattern;

said method comprising the steps of cutting out a bar-shaped subbase member as wide as one chip from the base member of said chip-like element, electrically connecting alternate ones of the electrodes along the thickness of said bar-shaped subbase member with each electrode pattern of said flexible board base member including a multiplicity of electrode pattern pairs by fixedly connecting said flexible board base member to the longitudinal side surface of said bar-shaped base member, and cutting out each multilayer electronic part from an integrated member of said bar-shaped subbase member and said flexible board base member.

9. A method of manufacturing a multilayer electronic part as described in Claim 8, characterized in that said manufacturing steps are carried out with other members attached to the upper and lower surfaces of the base member of said chip-like element.

10. A method of manufacturing a multilayer electronic part as described in Claim 8, characterized in that an insulative adhesive is filled in the minuscule gap between said bar-shaped subbase member and the base member of said flexible board with said

bar-shaped base member and said base member of said flexible board integrated with each other.

11. A method of manufacturing a multilayer electronic part as described in Claim 8, characterized in that each of said electrodes exposed to the long side surface of said bar-shaped subbase member is plated for connection assistance.

12. A method of manufacturing a multilayer electronic part as described in Claim 8, characterized in that an insulative pattern for cutting off the conduction between the adjacent electrodes along the thickness of the multilayer of said bar-shaped subbase member is formed on said flexible board.

13. A two-dimensionally arrayed element packaging structure characterized in that a plurality of electronic parts are integrated by being arranged in columns and rows in a two-dimensional array as a module, wherein each of said electronic parts is configured with a chip-like element having at least a surface electrode and a back electrode and a flexible board attached to one side surface of said chip-like element, the surface electrode and the back electrode of said chip-like element are electrically connected to a corresponding electrode pattern of said flexible board, and two electrode portions for external connection which are electrically connected to said surface electrode and said back electrode are formed of the electrode pattern of said flexible board or a

conductive portion connected with said electrode pattern.

14. A two-dimensionally arrayed element packaging structure as described in Claim 13, characterized in that each of said electrodes of said chip-like element and said electrode pattern of said flexible board are connected to each other by a thick-film conductive paste or a solder or an anisotropic conductive sheet.

15. A two-dimensionally arrayed element packaging structure as described in Claim 13, characterized in that said chip-like element is a single-layer structured element having only a surface electrode and a back electrode or a multilayer structured element having a surface electrode, an internal electrode and a back electrode.

16. A method of manufacturing a two-dimensionally arrayed element packaging structure, characterized in that only a plurality of acceptable ones of the multilayer electronic parts as described in any one of Claims 1 to 7 or only a plurality of acceptable ones of the multilayer electronic parts manufactured by the manufacturing method as described in any one of Claims 8 to 12 are integrated by being aligned in columns and rows thereby to complete a two-dimensionally arrayed module.

ABSTRACT

In order to provide a two-dimensionally arrayed probe (element packaging structure) in which a multilayer element can be used as a piezoelectric ceramic transducer element, each defective element can be replaced and the ill connection of each element can be repaired, and in order to provide a multilayer electric part suitable for realizing such an element packaging structure, the multilayer electronic part is configured with a multilayer chip-like element having a surface electrode, an internal electrode and a back electrode on the one hand and a flexible board attached to one side surface of the chip-like element on the other hand, alternate ones of the electrodes along the multilayer of the chip-like element are connected electrically to each other by the electrode pattern of the flexible board thereby to form two electrode groups, and the end portions of the electrode pattern of the flexible board are used as the two electrode portions for external connection which are electrically connected to the two electrode groups.

FIG.1

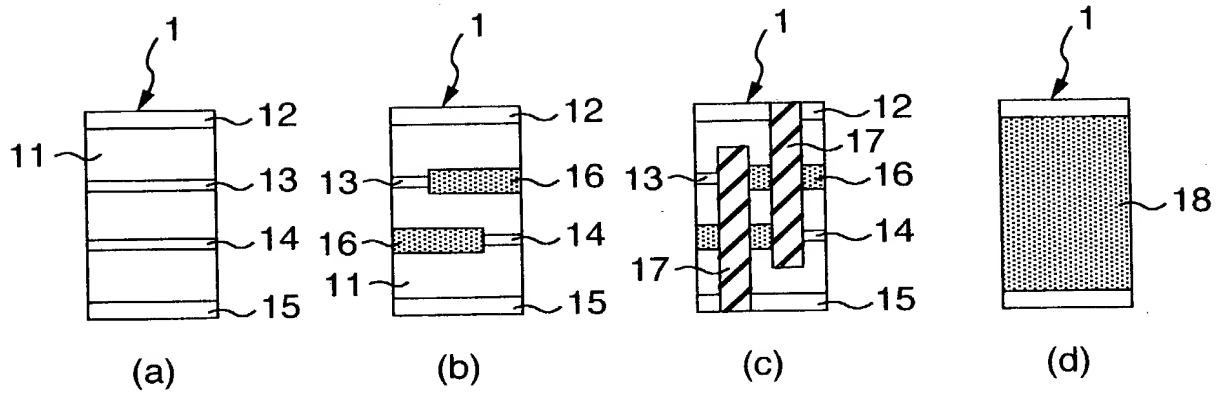

FIG.2

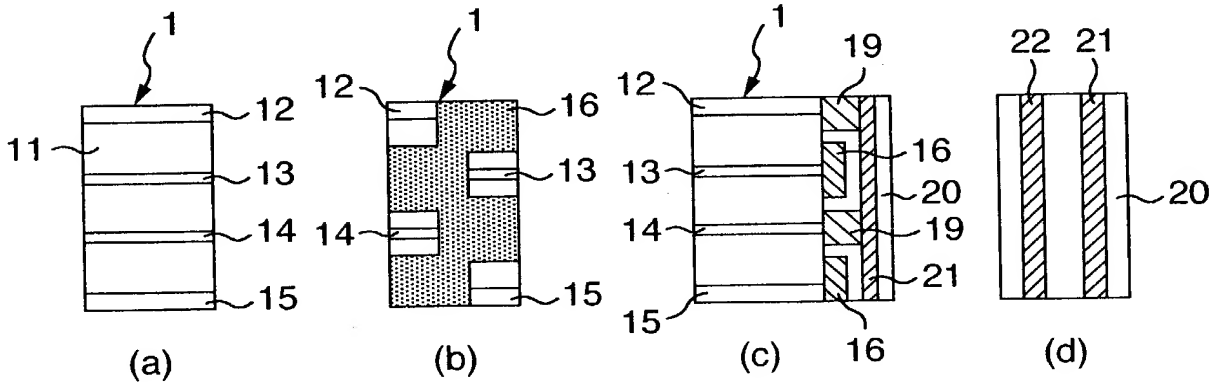

FIG.3

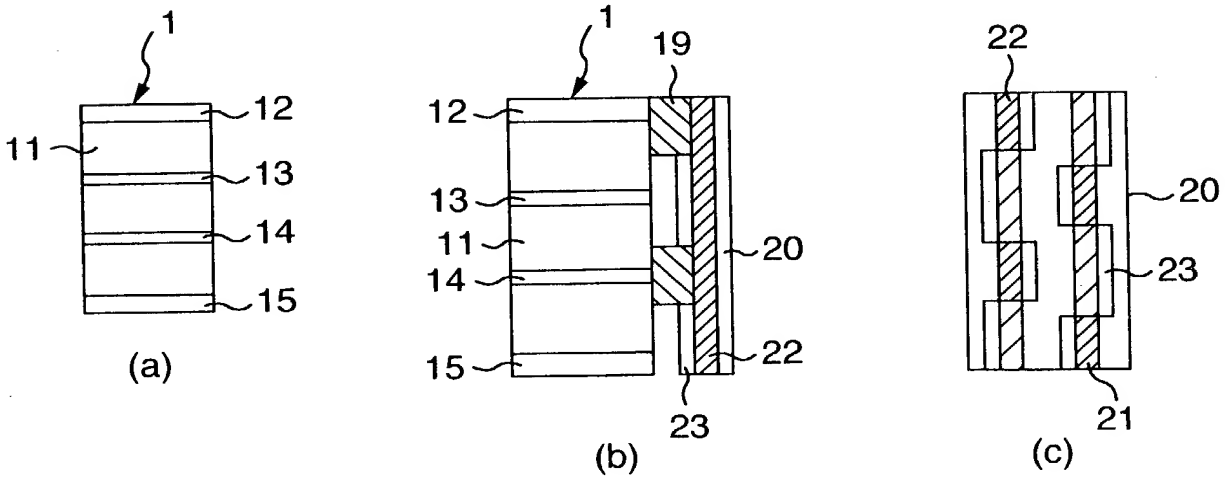

FIG.4

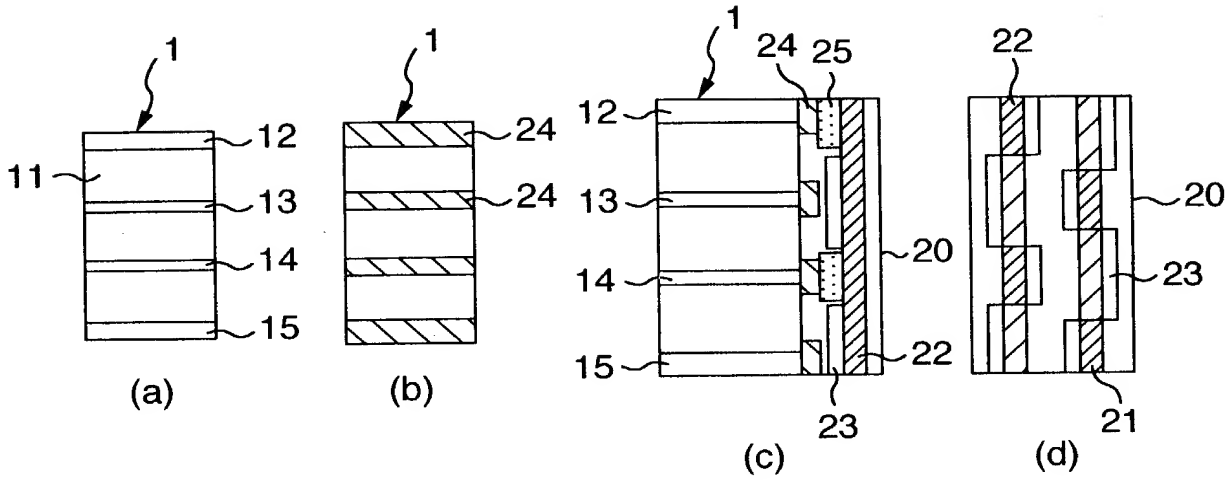
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FIG.5

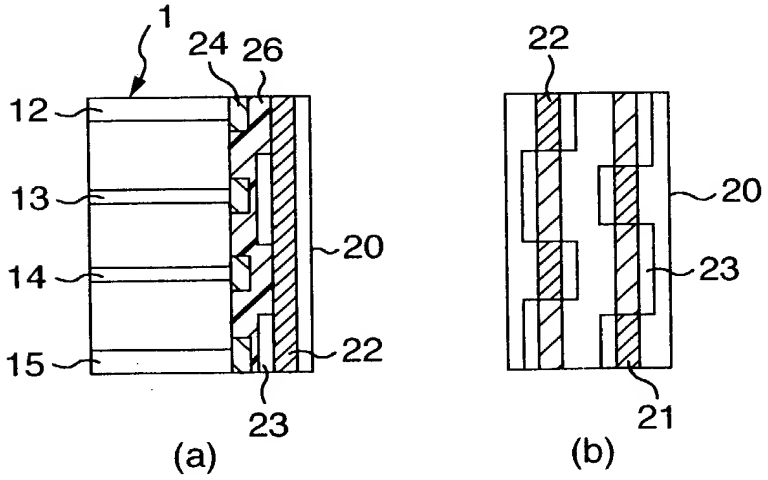
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FIG.6

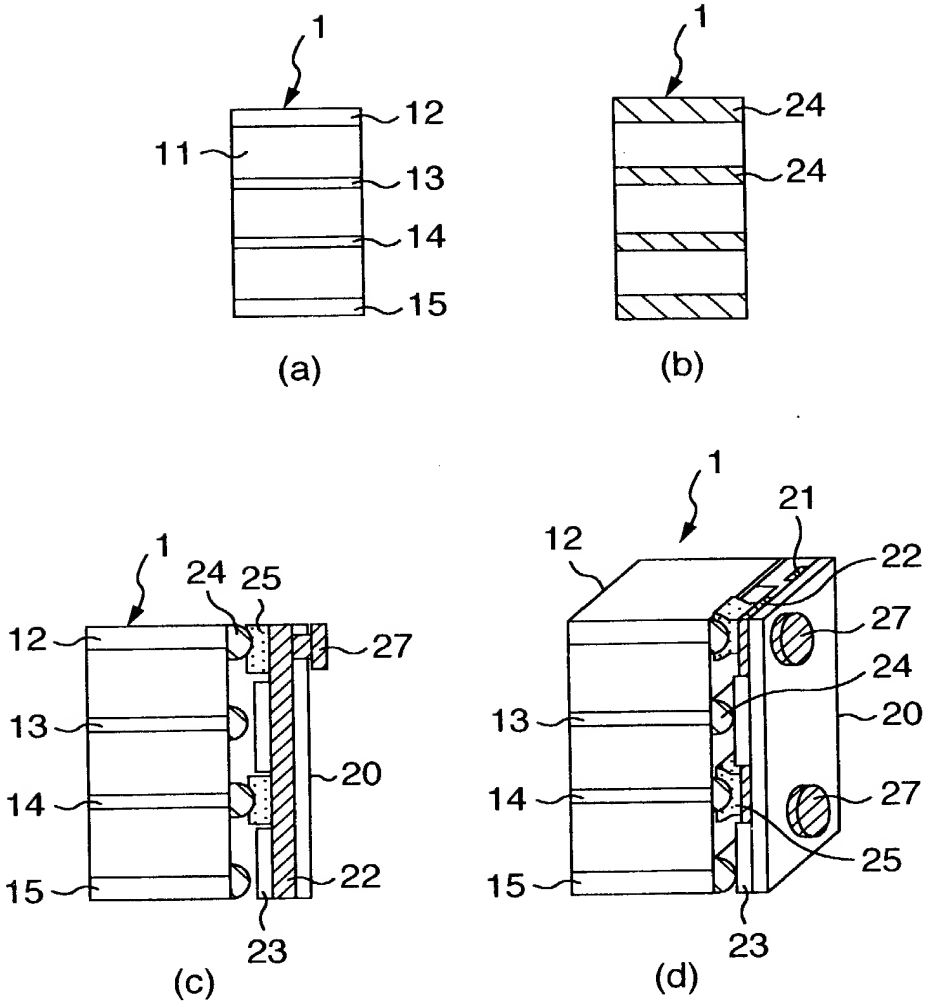
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FIG.7

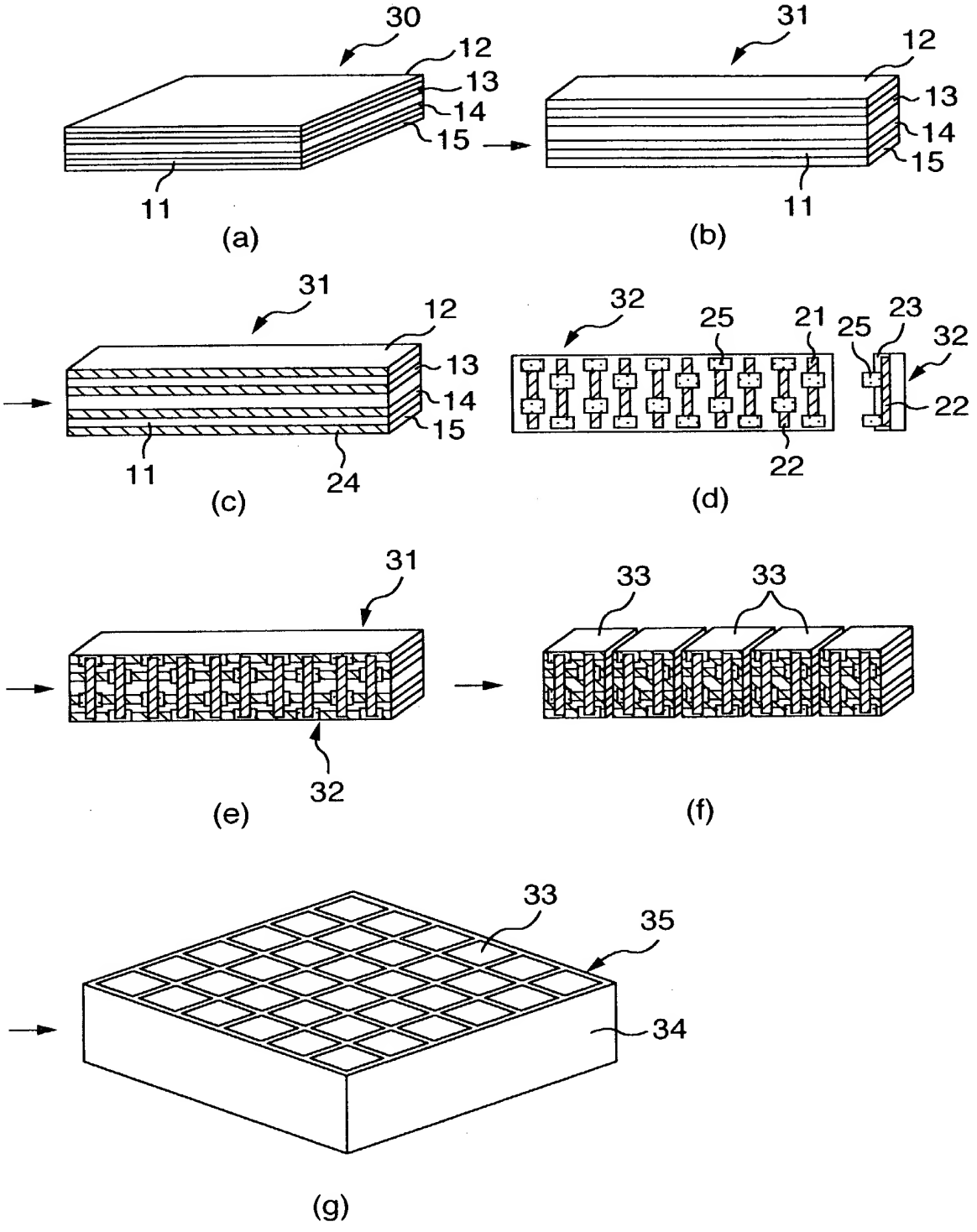
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FIG.8

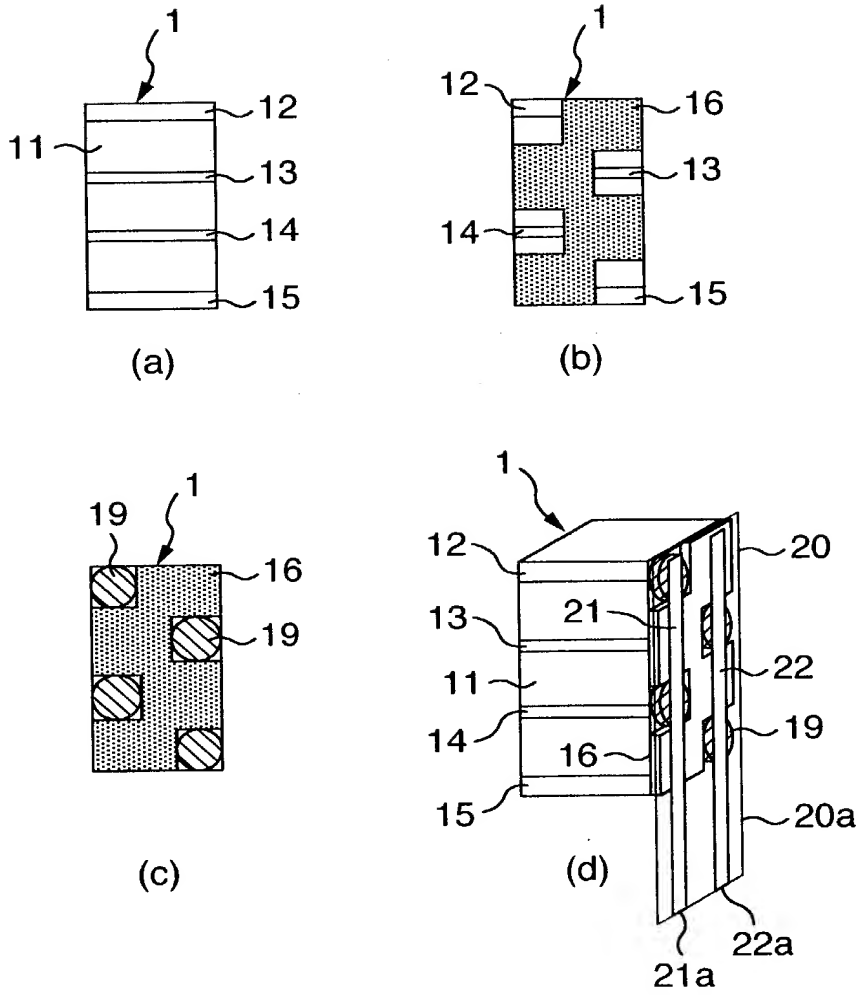
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FIG.9

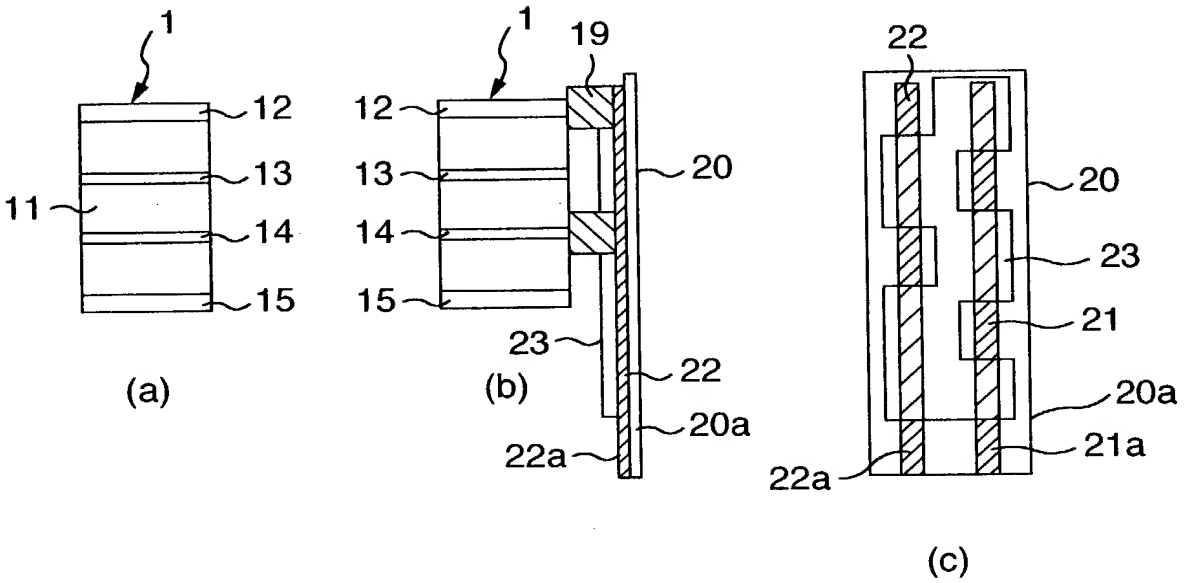
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FIG.10

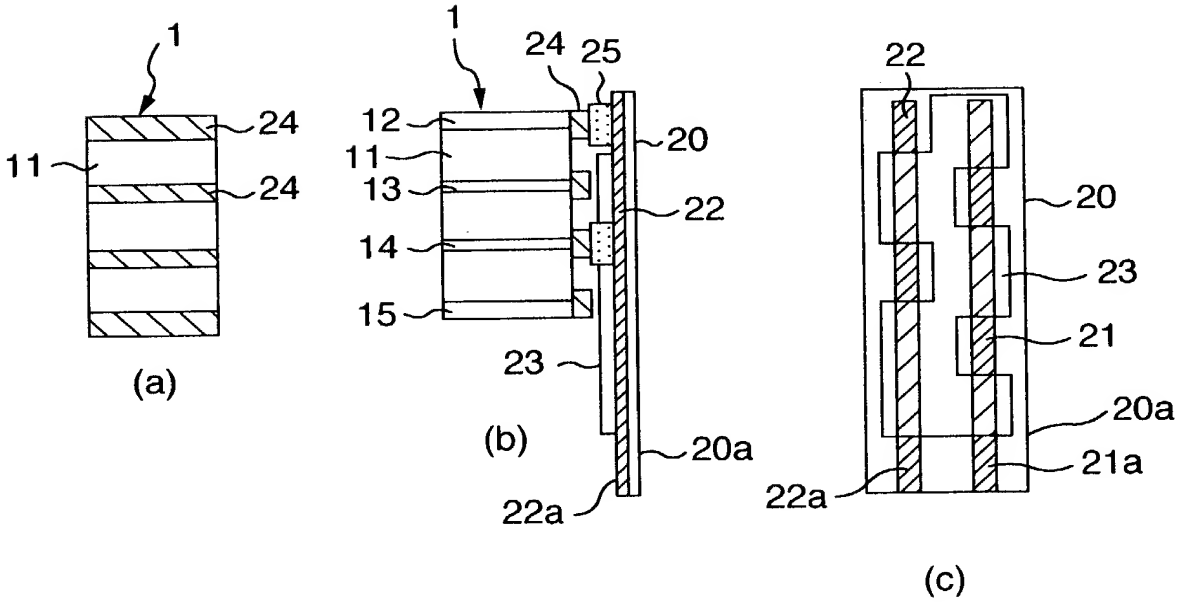
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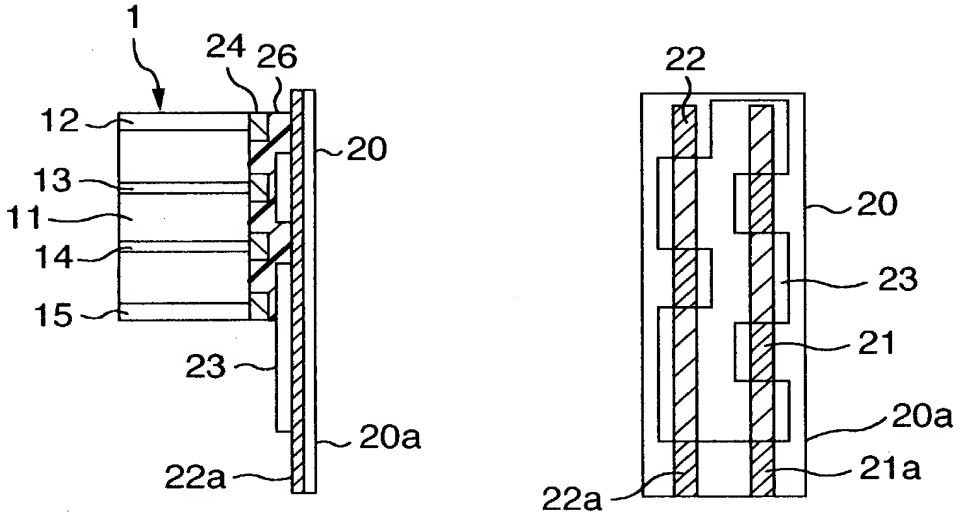
FIG.11



(a) (b)

FIG.12

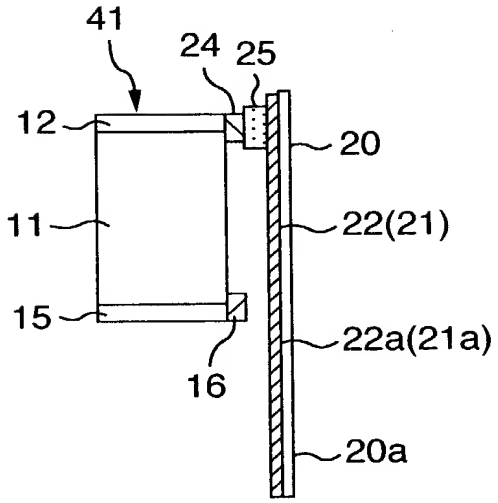

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FIG.13

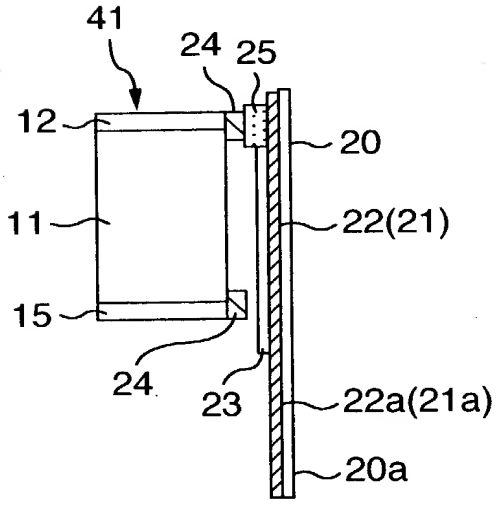
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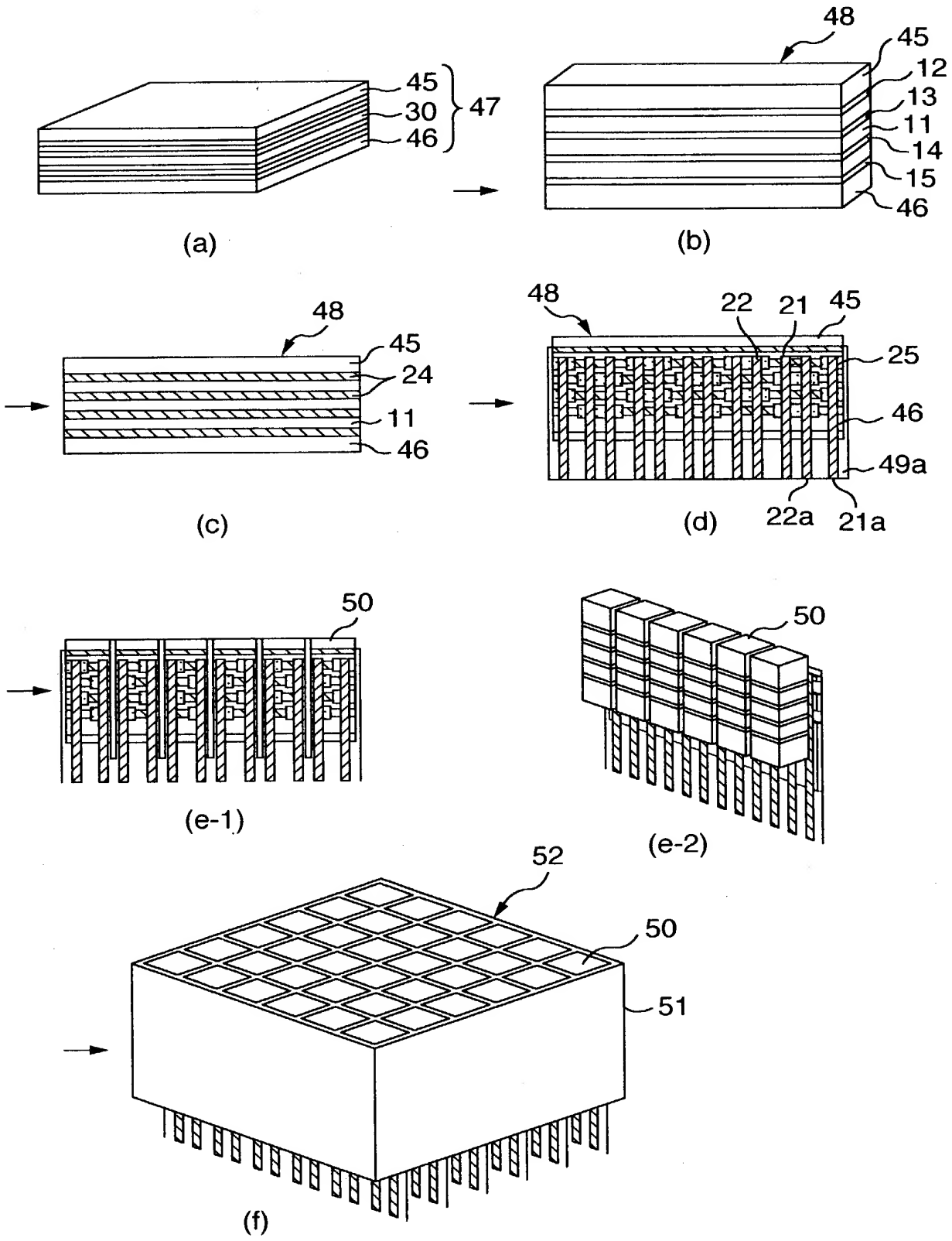
FIG.14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(f)

FIG.15

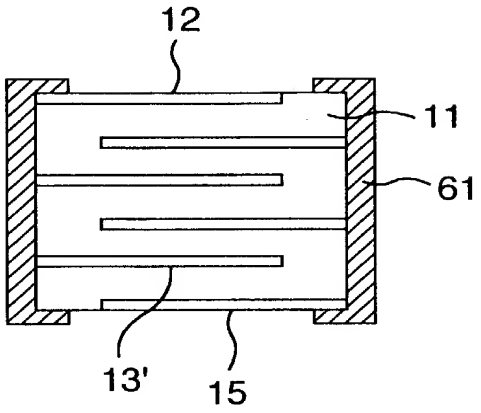
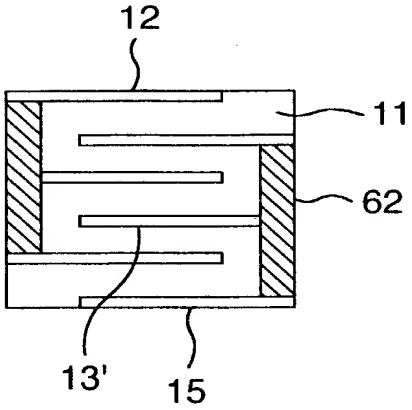


FIG.16



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First Named Inventor	ISHIHARA, et al.
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Examiner Name	
Attorney Docket Number	500.40053X00

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Date	April 24, 2001.

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Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

MULTILAYER ELECTRONIC PART, ITS MANUFACTURING METHOD, TWO-DIMENSIONALLY ARRAYED ELEMENT PACKAGING STRUCTURE, AND ITS MANUFACTURING METHOD

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following Box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
(該当する場合) _____に訂正されました。

☒ was filed on October 22, 1999
as United States Application Number or
PCT International Application Number
PCT/JP99/05848 and was amended on
_____ (if applicable).

☒ was filed on April 24, 2001
as United States Application Number or
PCT International Application Number
09/830127 and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条 (a) - (d) 項又は３６５条 (b) 項に基き下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約３６５ (a) 項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示している。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
10-308726	Japan	29/October/1998	☐
			☐

私は、第３５編米国法典１１９条 (e) 項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条 (c) に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）
POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

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発明者の署名	日付	Inventor's signature Date Shosaku Ishihara 6/22/01
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第六共同発明者	6-00	Full name of sixth joint inventor, if any Takaya OSAWA
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第八共同発明者		Full name of eighth joint inventor, if any
第八共同発明者の署名	日付	Eighth inventor's signature Date
住所		Residence
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私書箱		Post Office Address
第九共同発明者		Full name of ninth joint inventor, if any
第九共同発明者の署名	日付	Ninth inventor's signature Date
住所		Residence
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(第十以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for tenth and subsequent joint inventors.)